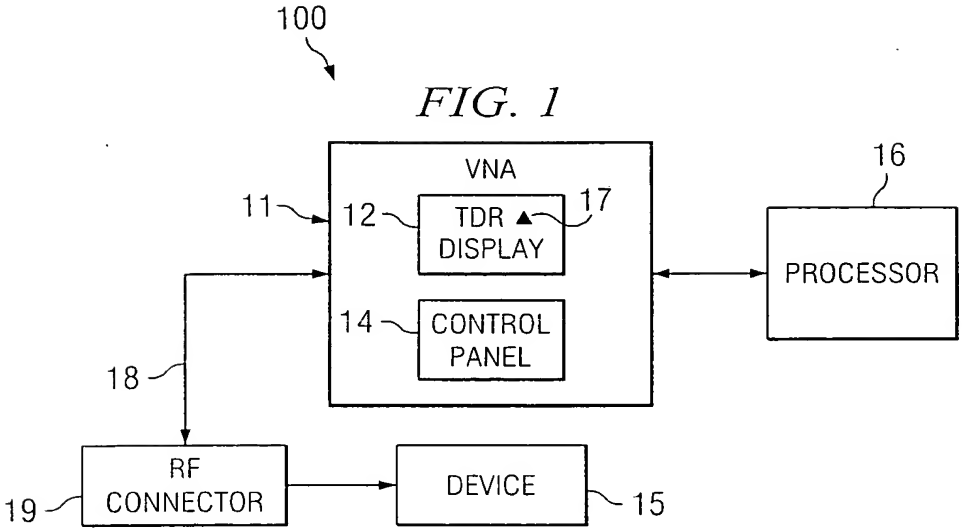

100
VNA
11
12
TDR
DISPLAY
17
16
PROCESSOR
14
CONTROL
PANEL
18
RF
CONNECTOR
19
DEVICE
15

FIG. 1

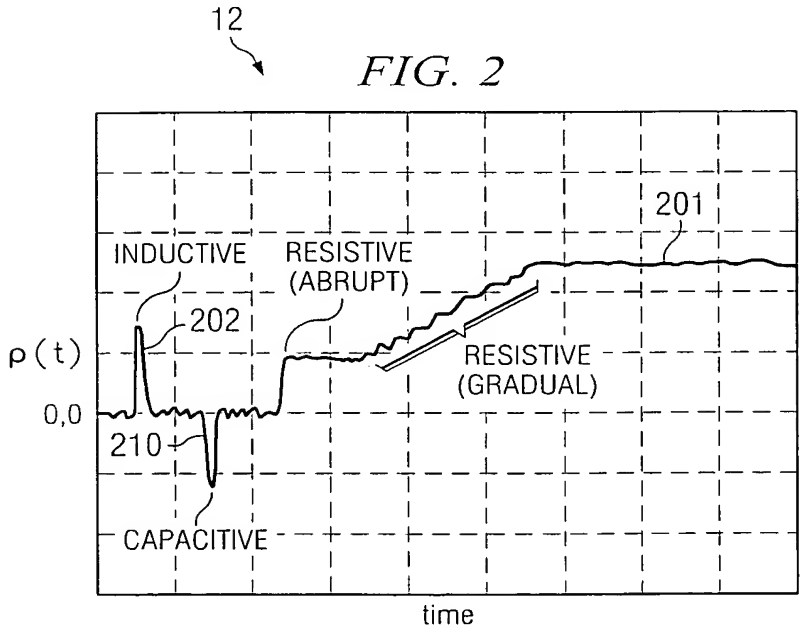

12
INDUCTIVE
RESISTIVE
(ABRUPT)
201
202
ρ(t)
RESISTIVE
(GRADUAL)
0,0
210
CAPACITIVE
time

FIG. 2

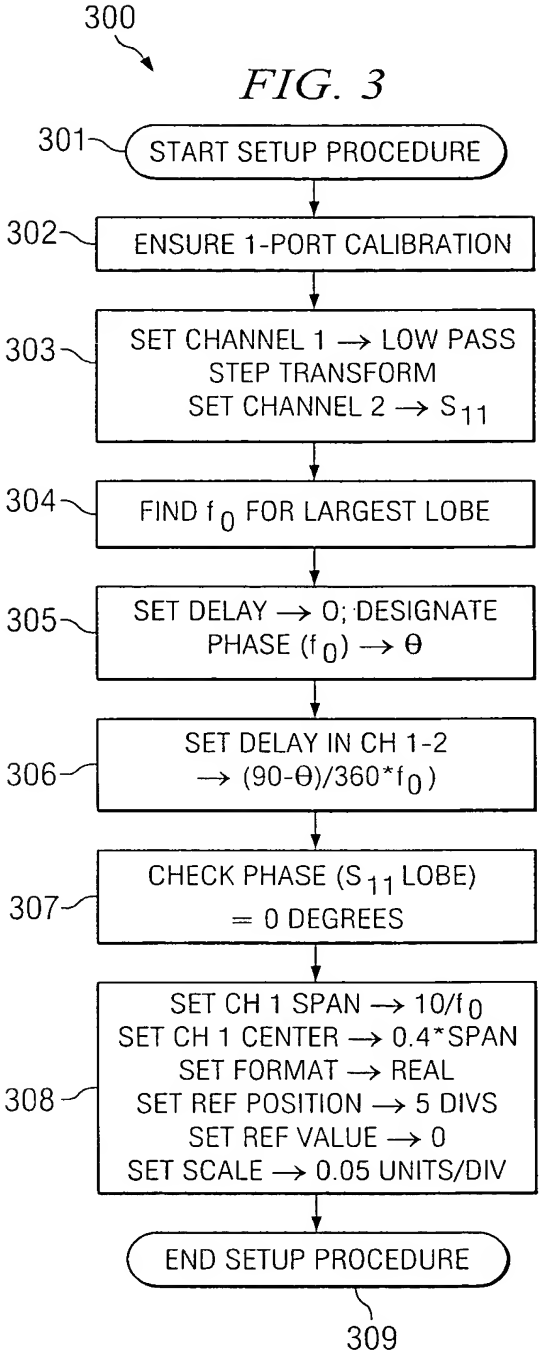

300
301
START SETUP PROCEDURE
302
ENSURE 1-PORT CALIBRATION
303
SET CHANNEL 1 → LOW PASS STEP TRANSFORM
SET CHANNEL 2 → S_{11}
304
FIND f_0 FOR LARGEST LOBE
305
SET DELAY → 0; DESIGNATE PHASE (f_0) → θ
306
SET DELAY IN CH 1-2 → (90-θ)/360*f_0)
307
CHECK PHASE (S_{11} LOBE) = 0 DEGREES
308
SET CH 1 SPAN → 10/f_0
SET CH 1 CENTER → 0.4*SPAN
SET FORMAT → REAL
SET REF POSITION → 5 DIVS
SET REF VALUE → 0
SET SCALE → 0.05 UNITS/DIV
END SETUP PROCEDURE
309

FIG. 3

FIG. 4

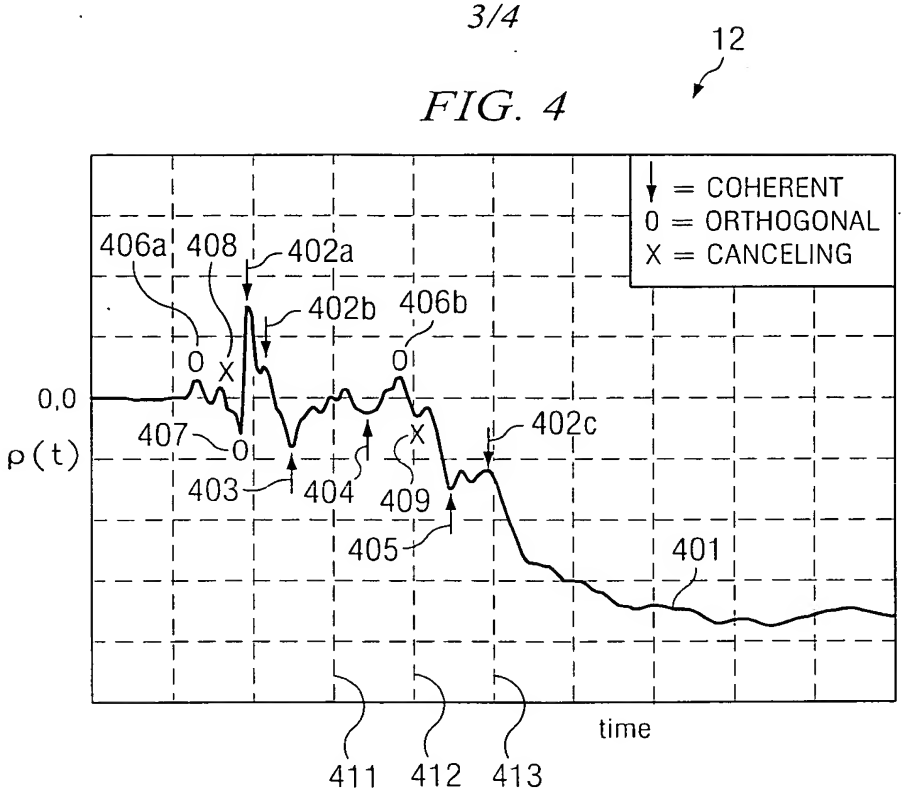
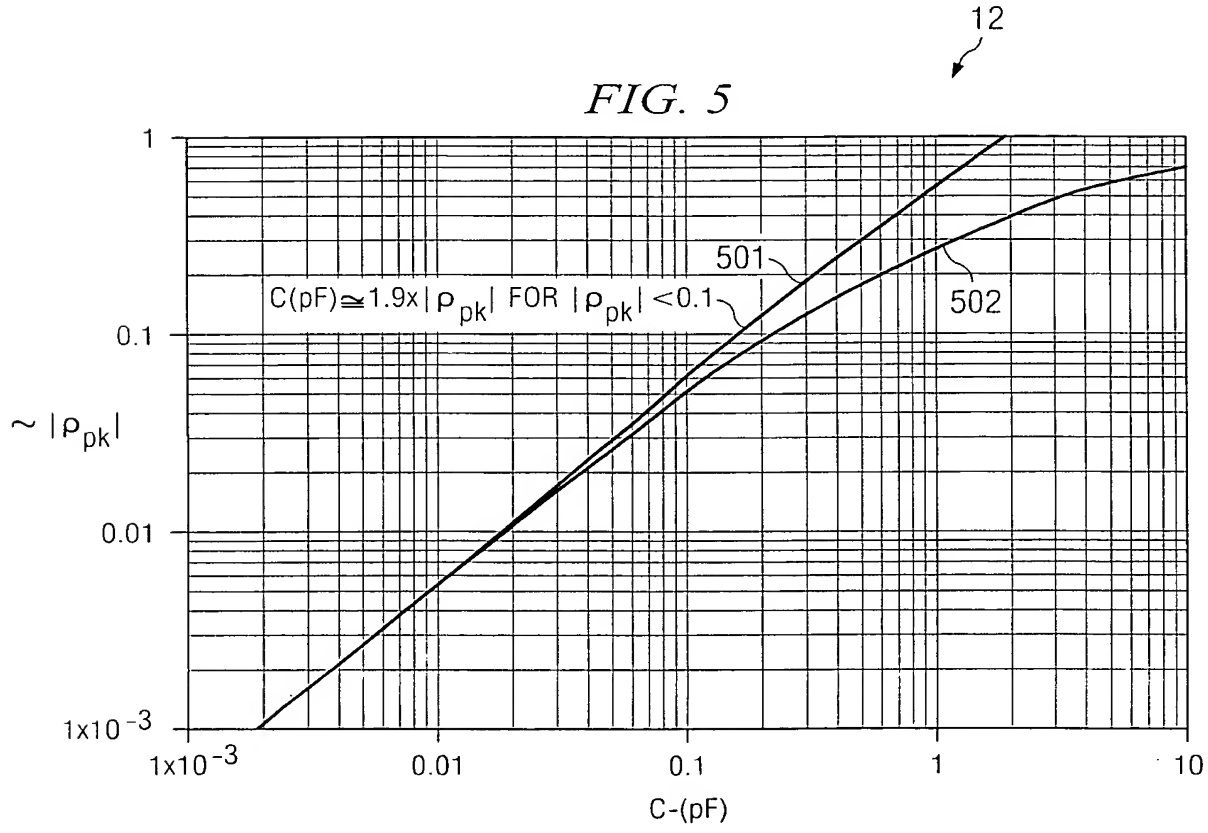
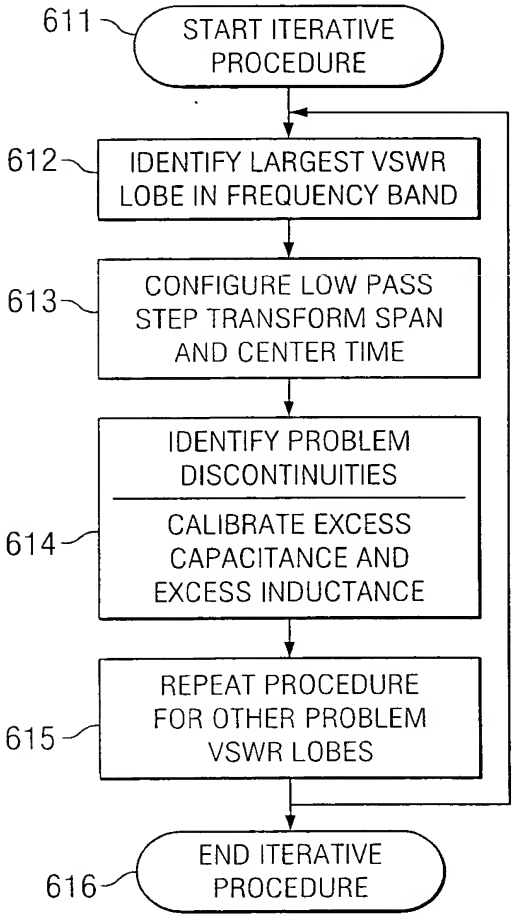

12
↓ = COHERENT
0 = ORTHOGONAL
X = CANCELING
406a
408
402a
402b
406b
0
X
0
0,0
ρ(t)
407
0
402c
X
403
404
409
405
401
time
411
412
413

FIG. 5


12
1
0.1
0.01
1x10⁻³
~ |ρpk|
C(pF)≅1.9x|ρpk| FOR |ρpk|<0.1
501
502
1x10⁻³
0.01
0.1
1
10
C-(pF)

610

FIG. 6A



600

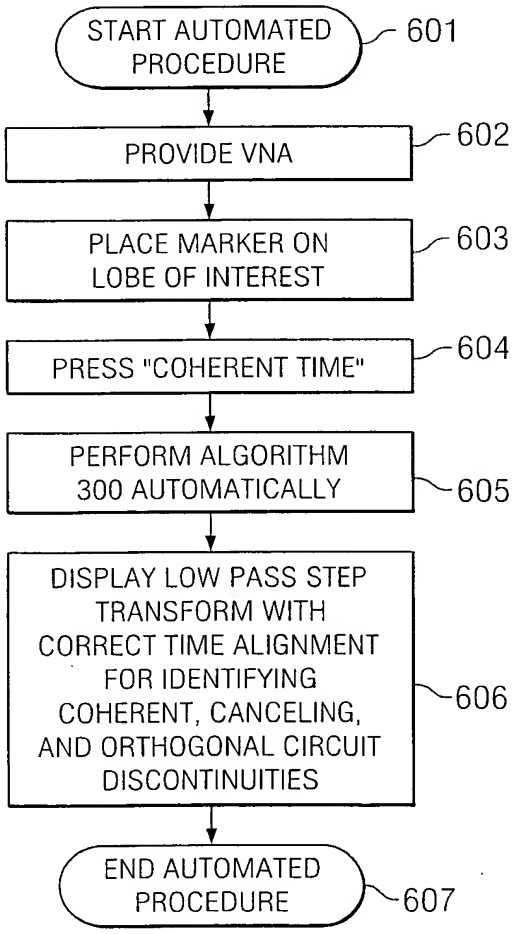



FIG. 6B